Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-13 (cancelled).

14 (currently amended): A control circuit of memory address decoding for determining whether a given address is located in one of a plurality of sections, each section having at least one memory unit ~~a plurality of memory units~~ and each memory unit having a unique corresponding address, the corresponding address using the binary system, the control circuit comprising:

an access module for receiving the given address;

a sorting module for making the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size, and if the size of a first section is equal to the size of a second section, the first and the second sections are capable of being swapped; and

a comparing module for building a bit-pattern for each section based on its corresponding addresses and sending a plurality of comparison signals after comparing the given address with those of each bit-pattern.

15 (original): The control circuit of claim 14 further comprising a logic module responsible for receiving the comparison signals and sending a decoding result to determine the given address is located in one of the sections.

16 (original): The control circuit of claim 14 wherein the sections are a plurality of memory modules.

17 (currently amended): The control circuit of claim 14 wherein the single bit-pattern is built for each ~~ssection inthe~~ section in the comparing module, the bit-pattern consisting of all common bits of the corresponding addresses in each section.

18 (currently amended): The control circuit of claim 14 wherein the comparing module comprises a plurality of comparing units, each comparing unit comprising a plurality of first level AND gates, a plurality of ~~XOR~~ NXOR gates, and a second level AND gate, each of the first level AND gates having two inputs for respectively receiving a mask bit generated from the bit-patterns and an associated bit of the given address, each of the ~~XOR~~ NXOR gates having two inputs for respectively receiving the output of one of the first level AND gates and a standard address generated from the bit-patterns, the inputs of the second level AND gate being connected to the outputs of the ~~XOR~~ NXOR gates and thereby sending out the comparison signals.

19 (new): A memory address decoding method for determining an objective section of a given address in a memory, wherein the memory is formed by at least one section with at least one memory unit, the method comprising:

assigning an address to each memory unit according to the memory size of the section;

obtaining at least one bit-pattern of each section according to the common rules of the bit of the addresses; and

comparing the given address with each bit-pattern to determine the objective section of the given address.

20 (new): The method of claim 19 wherein the section is formed by at least one memory module.

21 (new): The method of claim 19 wherein the addresses of the memory units located in

the section with greatest size are firstly assigned, and the addresses of the memory units located in the section with smallest size are lastly assigned.

22 (new): The method of claim 19 wherein the addresses of the memory units located in the section with greater size are smaller than the addresses of memory units located in the section with smaller size.

23 (new): The method of claim 19 wherein the bit-patterns are exclusive to each other.

24 (new): The method of claim 19 wherein the bit-pattern is obtained by all common bits of the address in each section.

25 (new): The method of claim 19 wherein the bit-pattern is obtained by partial common bits of the address in each section.

26 (new): The method of claim 19 the given address is located in the objective section when certain bits of the given address completely match the bit-pattern of the objective section.

27 (new): The method of claim 19 wherein the size of each section is a power of 2.

28 (new): A memory address decoding method for determining an objective section of a given address in a memory, wherein the memory is formed by at least one section with at least one memory unit, the method comprising:

sorting the sections according to the memory size of each section;

assigning an address to each memory unit of each section, wherein the addresses of the memory units located in the section with greater size are smaller than the addresses of memory units located in the section with smaller size;

obtaining at least one bit-pattern of each section according to the common rules of the bit of the addresses; and

comparing the given address with each bit-pattern to determine the objective section of the given address;

wherein if the memory size of a first section is substantially equal to a second section, the addresses of the first section and the section are swappable.

29 (new): The method of claim 28 wherein the section is formed by at least one memory module.

30 (new): The method of claim 28 wherein the bit-patterns are exclusive to each other.

31 (new): The method of claim 28 wherein the bit-pattern is obtained by all common bits of the address in each section.

32 (new): The method of claim 28 wherein the bit-pattern is obtained by partial common bits of the address in each section.

33 (new): The method of claim 28 wherein the given address is located in the objective section when certain bits of the given address completely match the bit-pattern of the objective section.